SIR ARTHUR LEWIS COMMUNITY COLLEGE

ENGINEERING AND THE CIRCULAR ECONOMY

ACADEMIC YEAR (2024/2025) – SEMESTER ONE

END OF SEMESTER EXAMINATION

TUTOR (S)	**:**	**Mr. Kendall Numa & Mr. Yoany Guerra Contino**
PROGRAMME TITLE	**:**	**Computer Systems Engineering Electrical Engineering**
COURSE TITLE	**:**	**Digital Principles & Technology**
COURSE CODE	**:**	**ELE211**
LEVEL	**:**	**Associate Degree/ Year Twos**
PAPER	**:**	**One**
DATE	**:**	**Tuesday, 10th December 2024**
COMMENCEMENT TIME	**:**	**9:00a.m.**
DURATION	**:**	**TWO (2) HOURS**
INVIGILATOR(S)	**:**	**T. Warner (Chief), J. E. Gaillard & K. O. Frederick**
ROOM(S)	**:**	**TRB-02-03**

GENERAL INFORMATION AND INSTRUCTIONS

- This paper consist of Two (2) Sections A and B. Answer questions on the foolscap paper provided.
- **Section A** consist of eight (8) questions. You are required to **answer ALL questions**.
- **Section B** consist of three (3) questions. You are required to **answer ANY TWO (2) questions.**
- The number in the brackets "[]" next to each question are the marks allocated.
- Students must sign **IN** and **OUT** on the examination class list.
- Students must **not** write their names on their answer sheets, only their ID number
- Please number your responses accurately.
- **Note: Bags, Books as well as writing paper not given by the invigilator should be deposited at the front of the examination room or as otherwise indicated.**
- **All cell phones must be turned off during the exam**

**DO NOT TURN THIS COVER SHEET UNTIL
YOU ARE TOLD TO DO SO!!!**

SECTION A - Answer all questions

Marks are awarded accordingly.

Question One

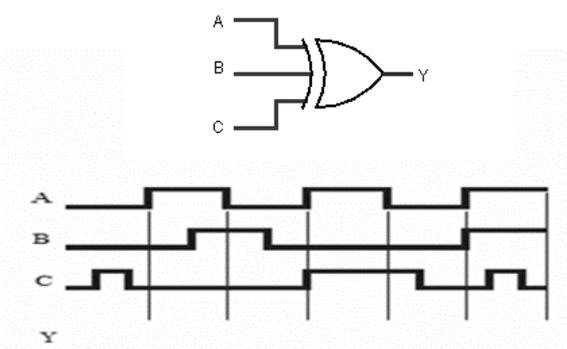
Complete the following table:

Inputs			Outputs		
A	B	C	OR	NAND	XOR
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

[3]

Question Two

Sketch the Y output for the diagram shown below.



[5]

Question Three

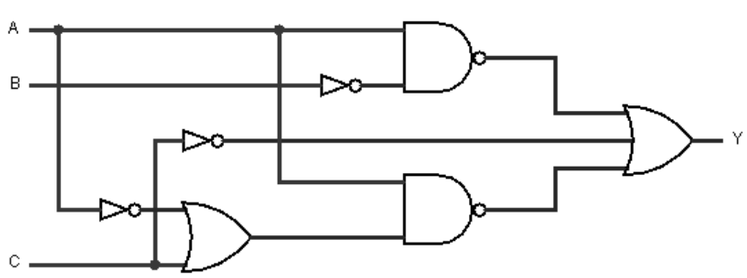
Draw the **logic circuit diagram** and **truth table** for the following Boolean expression:

$$X = \overline{A\bar{B} \cdot (A + C)} + \bar{A}B \cdot \overline{A + \bar{B} + \bar{C}}$$

[20]

Question Four

Write the Boolean expression for the logic circuit diagram shown below.



[5]

Question Five

Simplify the following Boolean expression using the rules and theorems of Boolean Algebra

$$X = \overline{A\bar{B} \cdot (A + C)} + \bar{A}B \cdot \overline{A + \bar{B} + \bar{C}}$$

[6]

Question Six

Simplify the following Boolean expression using the Karnaugh Maps Method.

$$X = \bar{A}\bar{B}\bar{C} + A\bar{C}\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C$$

[4]

Question Seven

Write the following expression in its Boolean form

$$F(w,x,y,z)=\sum(3,7,11,13,14,15)$$

[3]

Question Eight

Redraw the following circuit using only NAND Gates

[4]

[TOTAL 50 MARKS]

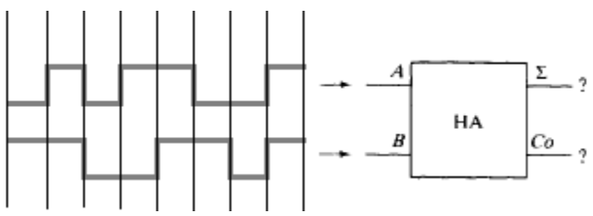
SECTION B – Answer Any Two Questions

Marks are awarded accordingly.

Question One

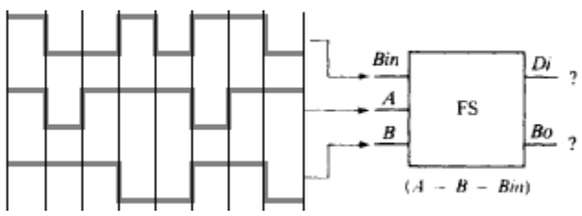
(A) Draw the truth table, logic circuit diagram and logic symbol for a full adder. [6]

(B) Determine the Σ and C_O outputs for the diagram shown below.



[4]

(C) Determine the Di and Bo outputs for the diagram shown below.



[4]

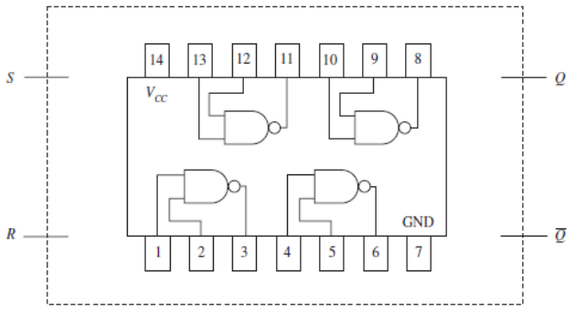
(D) Draw the block diagram of a 4 bit parallel adder using four full adders. [3]

(E) Draw the block diagram for the 7483 4-bit parallel adder IC [3]

[TOTAL 20 MARS]

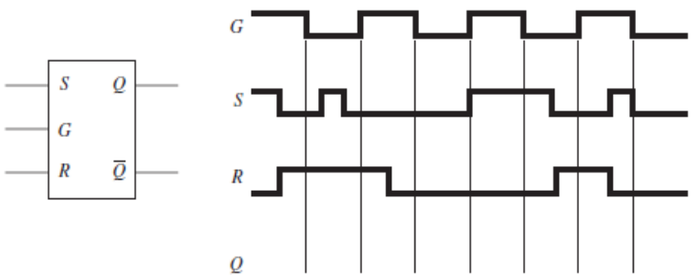
Question Two

(A) Redraw the diagram below showing the connections that need to be made to the 7400 quadruple 2- input NAND gate IC to form a NAND Gate SR latch.



[4]

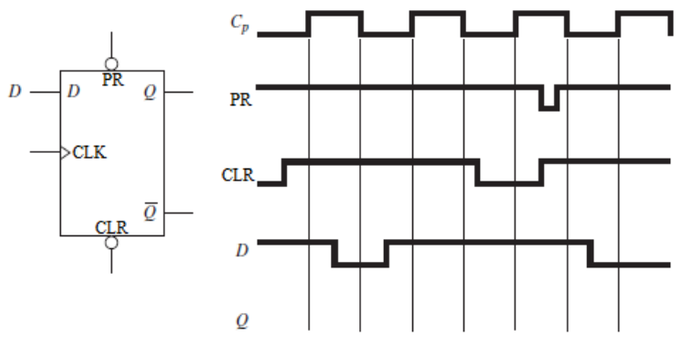
(B) Sketch the Q output for the diagram shown below.



[4]

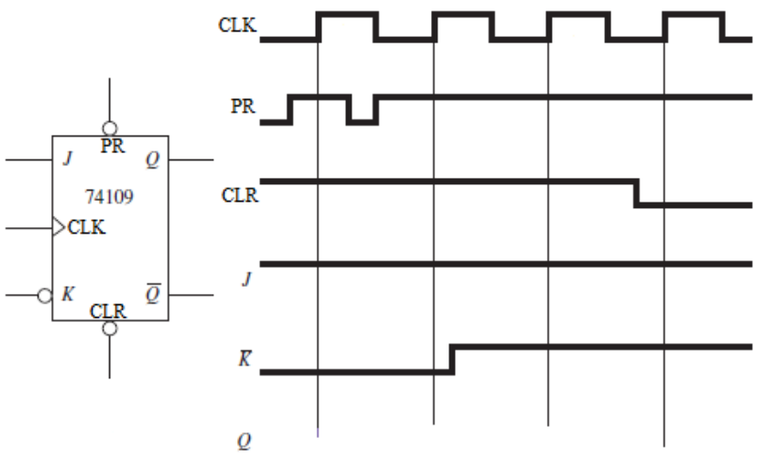
(C) Draw the circuit diagram for a D latch with enable using NAND Gates. [4]

(D) Determine the Q output for the diagram shown below.



[4]

(E) Determine the Q output for the diagram shown below.



[4]

[TOTAL 20 MARKS]

Question Three

(A) Name the four classifications of shift registers and draw the 4- bit variations of any two types. [8]

(B) Draw the circuit diagram for a ring counter. [2]

(C) Draw the timing diagram for CLK, Q_0, Q_1 and Q_2 for a 3-bit binary up counter for 10 clock pulses. [5]

(D) Design a MOD 11 ripple up counter. [5]

[TOTAL 20 MARKS]

END OF EXAM!